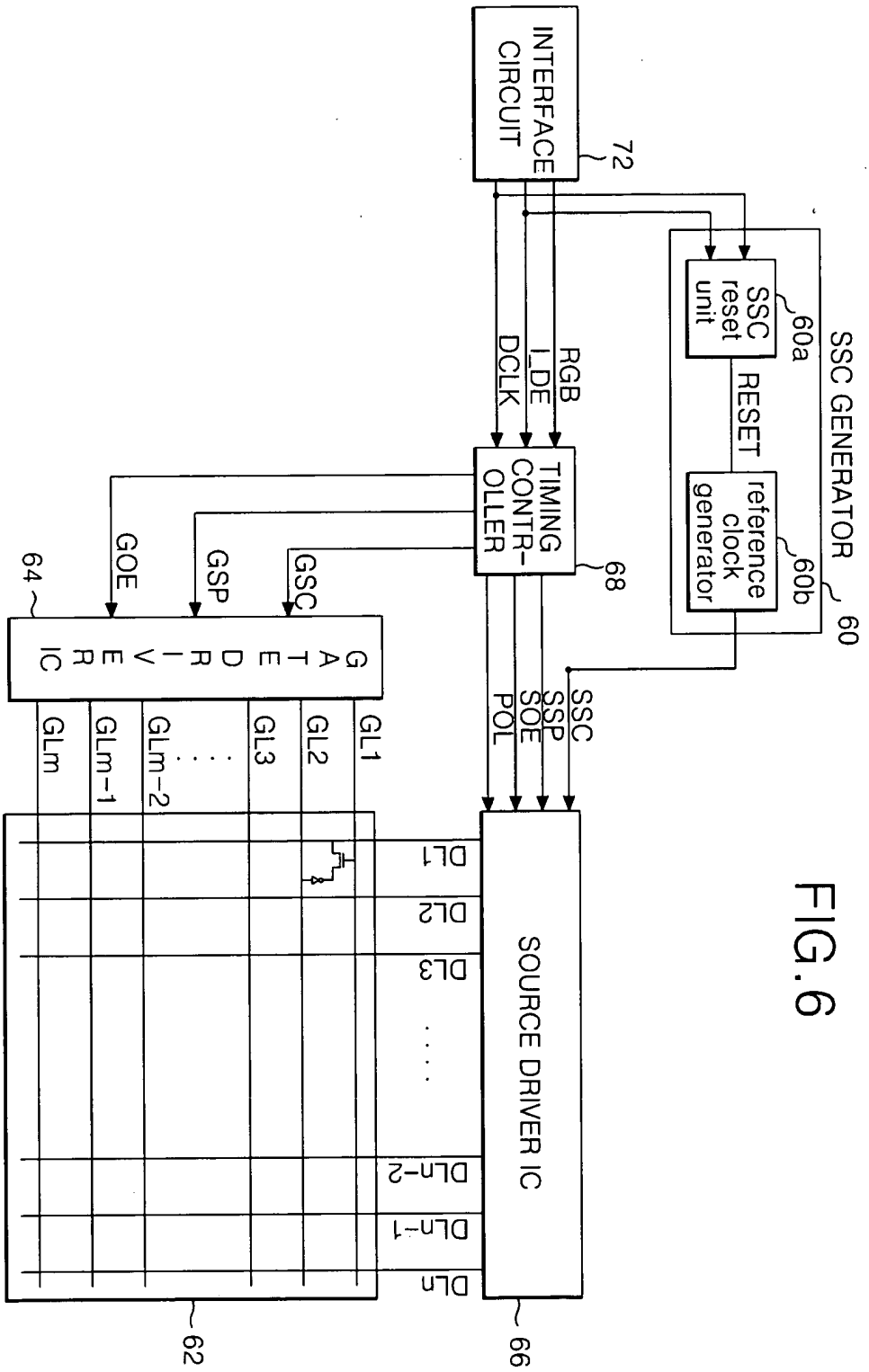
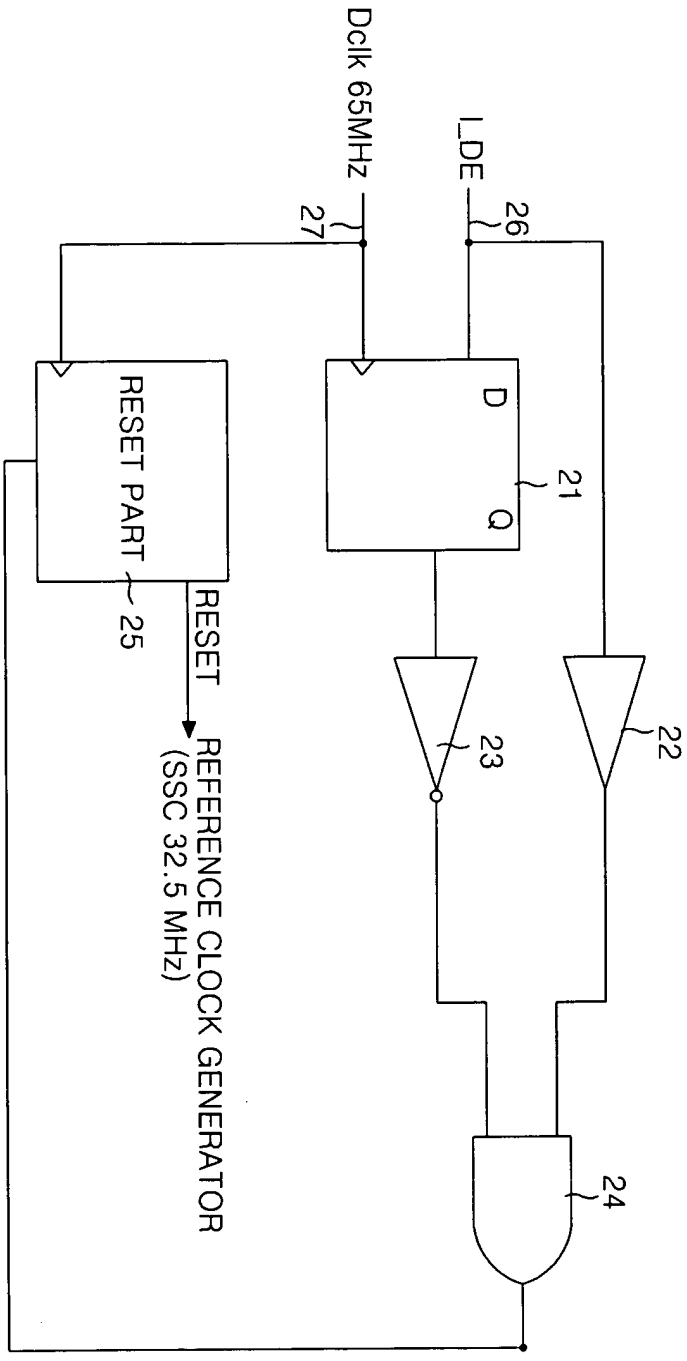

INTERFACE CIRCUIT
72
SSC GENERATOR
60
SSC reset unit
60a
RESET
reference clock generator
60b
RGB
I_DE
DCLK
TIMING CONTR-OLLER
68
GOE
GSP
GSC
64
GATE DRIVER IC
SSC
SSP
SOE
POL
GL1
GL2
GL3
GLm-2
GLm-1
GLm
DL1
DL2
DL3
DLn-2
DLn-1
DLn
SOURCE DRIVER IC
62
66

FIG.6

FIG. 7


Dclk 65MHz
27
I_DE
26
D
Q
21
RESET PART
25
RESET
REFERENCE CLOCK GENERATOR
(SSC 32.5 MHz)
22
23
24